ANALYSIS AND DESIGN OF DOUBLE TAIL COMPARATOR USING A LOW POWER GATING TECHNIQUES

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***Abstract*:**

Comparator techniques are the basic elements of designing the modern Analog and varied mixed signals systems. The speed and area is the main factors of high speed applications. Various types of dynamic double tail comparators is compared to an in terms of Delay, Area, Power, Glitches, Speed and average times. The accuracy of comparators is mainly defined by power consumption and speed. The comparators are mainly achieving by the overall higher performance of ADC. The High speed comparator is fully suffered from low voltage supply. Threshold voltage devices are not scaled at the same times, as the supply voltage of the devices. In modern CMOS technologies the double tail comparator is designed by a using the dynamic method it mainly reduces the power and voltages. The analytical expression methods it can obtain an intuitions about the contributors, comparators delay and explore the trade off dynamic comparator designs.

Keywords:

Double Tail comparator, Clock Gating, Power Gating, ADC, Dynamic comparator, Glitches

I. INTRODUCTION

Comparators have an essential influence of the overall performances in high speed analog to digital convertor (ADCs). In wide range of a comparator is a devices, which compares two currents or voltages and produces the digital output based on the comparisons. Since comparators are usually not used in the feedback there is not compensations, so neither the area reductions nor speed reductions value is invited.

Comparators is also known as 1-bit analog to digital converters and for that reasons they are mostly used in a large quantities in A/D converter, Dynamic comparators are most widely used in the designs of high speed ADCs. Due to the dynamic latched comparators are very attractive for many kinds of application, such as high speed analog to digital converters (ADCs). Increasing a packing densities coupled with a faster clock frequencies has forced the issues of heat removal and power dissipations to the front of virtually every main stream design applications. The problem is predicted to continue to be major challenges in the coming decades as we approach a Giga Scale Integration (GSI) [1].

Analog to the digital converters are the main building blocks of the most portable electronics equipments, such as a Mobile phones, Electronic products. They increasing demands of longer batteries life time of portable equipments has forced circuit designers to use a power supply voltages. However the supply voltages is lowered the performance of analog circuits is most degraded and the design of low voltage analog circuits become more challenging. The AX analog to digital converter are very suitable for low voltage application [2]. It consists of front end sampler regenerative stages, and a clocked amplifier to provide a small aperture times and high toggle rates. Then the clocked amplifier employs bandwidth modulation techniques that switching the feedback gain to reduce the reset time while keeping the high effective gain [3]. There are several fields of applications for comparator. In flash ADCs many clocked comparators decided in parallel for fast analog to digital conversions. So the demands on such comparators is mostly low power consumption and high sampling rates, while a small chip area is occupied. To have always the same capacitive loads at a both outputs of the comparators, the buffer has two parallel first stages; with the digital pin SW the second stages in the buffer can be switched. The buffer was designed with attenuations of two factors to enhance the bandwidth and to achieve a good linearity for the overall buffers [4].

Now a challenge to developed a new circuits structure that either avoids a stack of too many transistors between the supply rail, so that the technology given better ac performance not degrades or keep the advantages of standard circuits, a new latches for low supply voltage operations, where the advantages of a high impedance input, a rail - rail outputs swing, no static power consumptions [5]. This technique is a very suitable for very low power clocked and continuous time circuits such as level shifters, Op-amp and comparators. Design of a 10-bit Supply Boosted (SB) SAR ADC is presented as an example of the techniques. Voltage design techniques such as clock boosting were also used. A unique supplies and clock booster was designed as integral parts of a new supply boosted comparators. Input common range of SB comparators is extended by using supply boost level shifter circuits [6]. Among the key performance metrics of a dynamics latches used in a voltage comparators its input referred offset voltages. Relevant effect that contributes to the offset can be divided into static and dynamic component. The most commonly discussed source of static offset stems from threshold voltages mismatched in the constituent's transistors. Two simple equations for predicting the offset were derived and compared against simulation data's [7].

The degeneration resistors are the latching pair's and it's to reduce transistors charging times for regeneration. Charging times they allows most time for regeneration. The introductions method consists of the emitter degenerations resistor in the latching pairs. The degeneration resistor reduces the transistor charging times, providing more times for the critical process of regenerations. As the latching pairs are isolated from the input nodes degenerates still improved the sensitivity when a preamplifier is used [8]. To overcome the challenged associates with to reducing the supply voltages, a double tail latched comparators with variable capacitances, calibration techniques they used a metal oxide capacitors is implemented. An all digital time

domains delay interpolation techniques further enhanced the resolution with very little additional power consumptions [9].

II. CONVENTIONAL DYNAMIC COMPARATOR

The double tail comparators achieved the better performances and the double tail comparator and the architectures it mainly used in the better performances used in the low voltage applications. The comparators designs based on the double tail architectures. The main idea of this method is to increases ΔVfn/*fp* is to increase the latch regenerations speed. The main operations of the comparator is during reset phase CLK = 0, Mtail1 and M tail2 is OFF, to avoiding these static powers, M3 and M4 switches pulls both fn and fp nodes to VDD. Hence the transistors Mc1 and Mc2 are cut off, intermediate stage transistor MR1 and MR2 is reset both latches outputs to ground. During decision making phase CLK = VDD. Mtail1 and Mtail2 are on transistors M3 and M4 turn OFF. Further, at the beginning of the phase, the control transistors are still off. Thus, fn and fp starts too dropped with different rates an according to the input voltages. The second terms, t latches, is the latching delay for two cross coupled inverters. It is assumed that a voltage swings of Vout = *V*DD/2 has to be obtained from an initial output voltage differences V_0 at the falling output. This is a self biasing differential amplifier. An inverter was added at the outputs of the amplifier as additional gain stages, to isolate any load capacitances from the self biasing differential amplifier.

The size of M_1 and M_2 are settled by considering the differential amplifier's Trans conductance and the input capacitance. The Trans conductance sets of the gain of the stages while the input capacitance of the comparator is determined by the size M1 and M2. Similar to the conventional dynamic comparators, the delay of these comparators comprised two main parts, t_0 and t latches. The delay t_0 represents the capacitive charging of the load capacitance CL out (at the latch stage output nodes, out_n and out_p) until the first n channel transistors (M_9/M_{10}) turns on, after which the latch regeneration starts; thus t_0 is obtained where IB_1 the drain current of the M_9 and approximately equal to the half of the tail current. Thus it can be concluded it's two main parameters which influences of the initial outputs differential voltages and thereby the latch regenerations times are the trans conductance of the intermediate stages of the transistor (gmR_1,2) and the voltage differences at the first stage outputs (fn and fp) at time t_0.

III. PROPOSED DOUBLE TAIL COMPARATOR

To achieve the better performances of double tail architectures in low voltage applications, the proposed method comparator is designs based on the double tail structure.

Operation of Proposed Comparator

1. Reset Phase: Clk = 0, $Mtail_1$ and $Mtail_2$ OFF. For this process static power is avoided. np and nf nodes to VDD. Latches to be Ground.
2. Decision making phase: C_{lk} = VDD, $Mtail_1$ and $Mtail_2$ are ON state, M3 and M4 OFF state.

During reset phase Clk = 0, $Mtail_1$ (M3) & $Mtail_2$ (M 20) is OFF, M10 & M13 will pull both fn & fp nodes to VDD. Hence MC (M11) & MC (M12) are cut off M6, M9 are discharged to output nodes to VSS. During an decision making phase Clk = VDD, Mtail1(M3) & Mtail2 (M20) are ON, transistor M_{10} & M_{13} will be OFF and fn & fp nodes are start drop with different rates according to input voltages. VINP>VINN means fn is faster than fp, M15 transistor provides more current than M14. MC (M_{11}) is turn on, fp node pulling back to VDD MC (M12) remains OFF, f_n node discharged. Offset will low and delay reduced. Parallel connected dynamic latches is used as load of first stages to increase the voltage difference between due to cascade connections delay will more compared to parallel connections.

The latch of this first stages start regenerating depending on the input differential voltages (Vin1, Vin2), producing a large difference voltage. This difference voltages is sensed at the second stage inputs and the second stage latch regenerate outputs voltage Out1 and Out2. As fast sensing it is exploiting less time to produces output when comparing to previous works. It consumes less power compared to conventional one. As the way the delay has been reduced.

IV. EXPERIMENTAL RESULTS

Existing Model:

In order to compare the proposed model comparator with the conventional and double tail dynamic comparator all circuits have be simulates in 140nm CMOS technology, as the part of post layout simulations have been simulated in Tanner EDA tools, which is used to be calculates the area of the conventional dynamic comparators as shown in Fig 1, Double tail dynamic comparators in Fig.3 and proposed double tail dynamic comparator.

Circuit Diagram

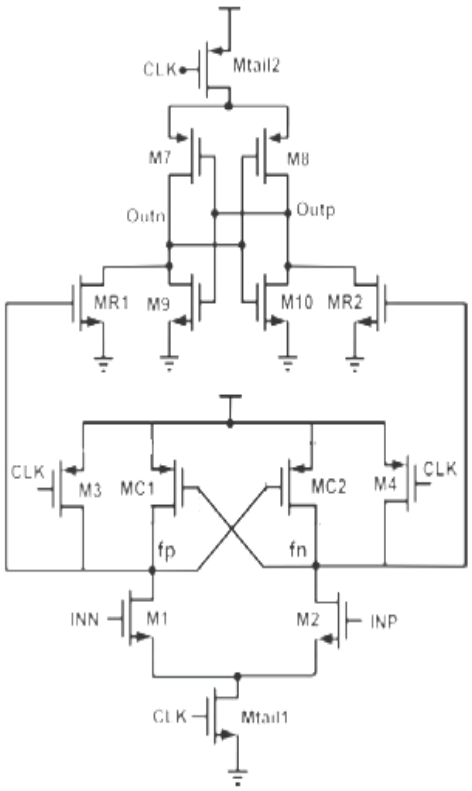

Fig .1 Existing model Dynamic Comparator

Due to the fact that of the parasitic capacitances of input transistors, do not directly affects the switching speed of the output nodes is possible to designs the large input transistors to minimize the offsets. The disadvantages, on the other hand, are the fact that due to several stacked transistors, sufficiently high supply voltages is needed for a proper delay times. The reason is that at the beginning of the decision, only transistors *M*3 and *M*4 of the latch contribute to the positive feedbacks until the voltage levels of the one output node has dropped below the level small enough to turn on transistors M_5 or M_6 to start complete regenerations.

Graph Output:

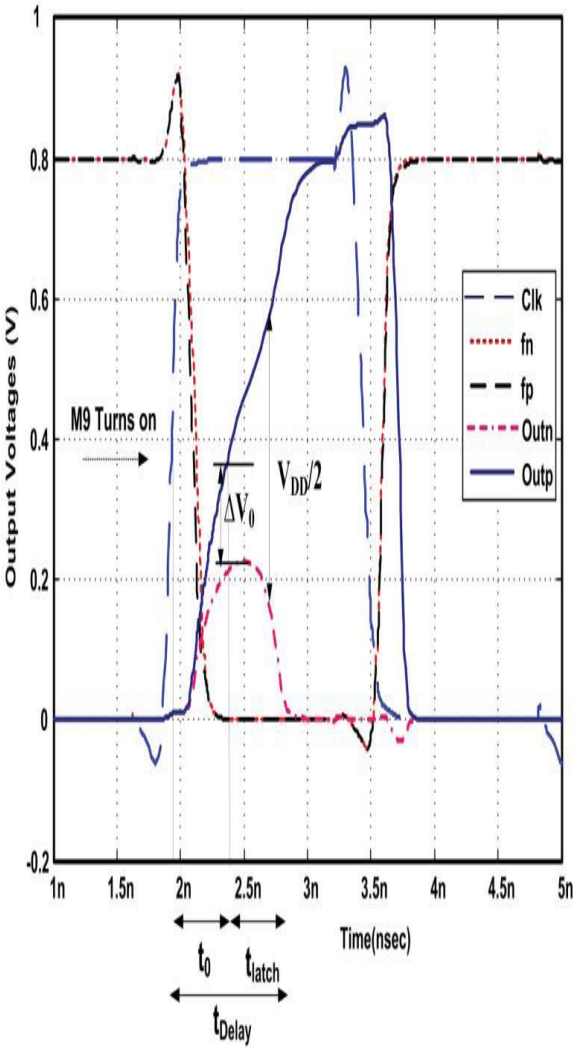

Fig.2 Energy diagram of existing system

Proposed Method:

As long as fn continuously falling, the corresponding PMOS control transistors (*M*c1 in this case) starts to turn on, pulling fp nodes back to the *V*DD; so another control transistors (*M*c2) remains off, allowing fn to be discharged completely. In other words unlike conventional double tail dynamic comparators which in *V*fn/fp is just a functions of input transistors transconductance of input voltage difference in the proposed structures as soon as the comparator detects for the instance nodes fn discharging faster, a PMOS transistors (*M*c1) turns on, pulling the other nodes fp back to the *V*DD.

Circuit:

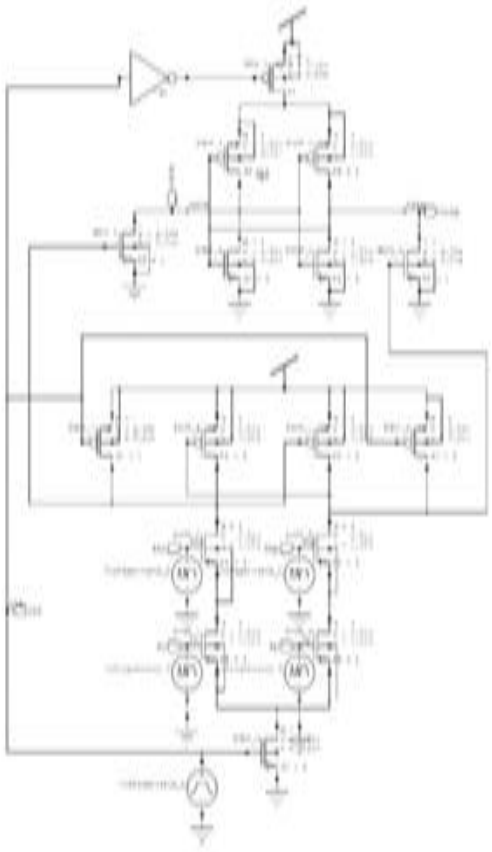

Fig 3 Proposed Model Circuit

Therefore the time passing, the difference between the fn and fp (*V*fn/fp) increases in a exponential manner, leading to the reductions of latch regeneration times.

In this evident that the double tail comparator technologies can operates faster and be used in lower supply voltages, while consuming nearly the same powers as the conventional dynamics comparator. In case of even much better for the proposed comparator when compared to the conventional doubletail topology.

Parsing	0.9 seconds
Setup	0.02 seconds
DC operating point	0.00 seconds
Transient Analysis	1.13 seconds
Overhead	2.00 seconds
Total	3.20 seconds

Simulation Graph:

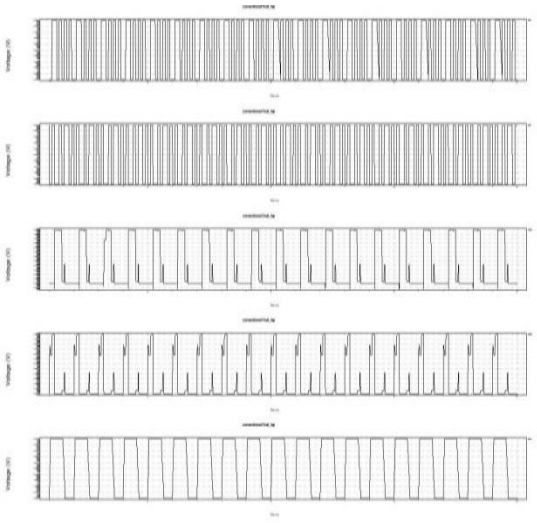

Fig4 Proposed Output

VI. CONCLUSION

This works presenting that comprehensive delay of analysis for clocked dynamic comparator. Two common structures of conventional dynamic comparators and conventional double - tail dynamic comparators have been analyzed. New dynamic comparator with a low voltage and low power capabilities has been proposed in order to improve the performance of the comparators and also reduces the delay. The estimated area is evaluated in using post layout simulations with the help of micro wind simulators.

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