DESIGN OF MODIFY WILSON CURRENT MIRROR CIRCUIT BASED LEVEL SHIFTERS USING STACK TECHNIQUES

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Abstract — Wide Range of level Shifters is fast energy efficient converters capable of converting the low voltages to high voltage. Level Shifters are mainly used to shifting their voltage from one level to other levels. Multi voltage systems utilize the advantage of level shifters. Multi voltage systems consist of low voltage as well as high voltage. Existing methods was implemented by using the LVT (Low Threshold Voltage Transistor) which produces the leakage power dissipations. Proposed method is implementing by using the forced PMOS method to reduce the leakage powers. Usually LS are inserted only while crossing low voltage domains to high voltage domain. In this paper modified the Wilson current mirror based level shifter is designed by using stack techniques. Measurement results were demonstrated by using cadence Tools.

Keywords— Level Shifters, Multi voltage systems, Widlar Wilson Circuits, Forced PMOS technique.

I. INTRODUCTION

The growing market of mobile batteries power electronic systems (e.g., cellular phone, personal digital assistant, etc.) Demand the designer of microelectronics circuits with low power dissipation [1]. More generally density, size and complexity of the chips continues to increase the difficulties in providing to adequate the cooling might either’s add significant cost or limits the functionalities of the computing system which make use of those integrated circuit. In the past years, several techniques methodologies and tools for designing a low power circuits have been presented. However, only few of them have found their ways in current design flows [2].

The major three major sources of power dissipation in a CMOS circuits. These are switching short circuit power and leakage power. Switching power is mainly due to charging and discharging capacitors driven by the circuits. Short circuit powers are mainly caused by the short circuits current that arise when pairs of PMOS/NMOS transistors are conducting simultaneously [3]. Finally leakage power originated from substrate injections and sub threshold effect. One of the main reason causing from the leakage power increases is the increase of sub threshold leakage powers. When a technology feature size scales down suddenly supply voltage and threshold voltage also scale down. Sub threshold
leakage power increases exponentially as threshold voltage decreases. Stack method forced NMOS, Forced PMOS and sleepy keeper method are the some of the leakage current reduction methods [4].

II. LEVEL SHIFTERS

A. CONVENTIONAL LEVEL SHIFTER

A Sub threshold LSs are surveyed in their section. Conventional cross coupled LS are differentially cascade voltage switch logic (DCVSL) for raising a low voltage level, as shown in figure.1. The drive strength of NMOS transistors is enhanced to overcome the leakage of weakly conducting PMOS transistors. The operating range of CC LS depends on the transistor threshold voltages (\(v_t\)) and size; however, the operating range of CC LSs is very difficult to extend the sub threshold region (with respect to NMOS \(v_t\)) because of the NMOS drive strength decreases exponentially. For a converting sub threshold voltage, CC LS requires an exponentially increased in NMOS transistor size [5,6].

![Figure 1. Conventional Level Shifter](image)

B. Current Mirror based Level Shifter

Fig.2 shows conventional level shifters that use a basic current mirror circuit. The conventional current mirror level shifter can converts a deep sub threshold level because a high drain to source voltage of PMOS transistor facilitate the constructions of a stable current mirror, which offers an effective ON - OFF current comparison at the output nodes. However, a high amount of Quiescent current occurred when the input voltage is high threshold. These high power consumptions limit the use of the conventional Current Mirror Level Shifter [7].
B. WILSON CURRENT MIRROR BASED LEVEL SHIFTER

Fig.3 shown a CM-type LS that uses a Wilson Current Mirror (WCM), which clamps the quiescent power consumptions under a super threshold input.

A two stage CCLS of Pull up driving strength is reduced by their header NMOS, which expands the convertible input voltages. In shows that CC-type LS (CCPNR), which the output stage is a part of their NOR gate. The primary input is accelerating to the overall LS speed. It uses Logic Error Correction Circuit (LECC), it monitors input and output updating data during the pulse. The MWCMHB LS is a hybrid structure of comprising a modified Wilson current mirror and CMOS logic gates [7]. The input and output level ranges from a sub threshold voltage to their standard supplies voltage defined in a transistor technology. A Bidirectional level conversion is available; that is input and output levels can be scaled independently.
C. MODIFIED WILSON CURRENT MIRROR BASED LEVEL SHIFTER

The MWCMHB LS structure is illustrated with three circuit blocks, as shown in Figure 4. A Modified Wilson Current Mirror Circuit (MWCM) is located in Block 1. When VDD1 is a sub threshold and VDD2 is high, the MWCM structures balanced the rising and falling delay at node A, without losing the original statics bias is favored in the WCMLS [4]. However, when the VDD1 and VDD2 levels are closed, the MWCM encountered the same problems as the WCM. The cascade PMOS has been insufficient drives currents and increasing the rising delay.

Therefore in a block 3 delay path is designs with an adaptively to reducing the rising delay and maintained at moderate duty cycles. Output inverters offered with sufficient drives strength, which is required into a standard cell designs. Unlike the CCPNR level shifter, which has similar structures, the proposed level shifters uses a CM type of amplifiers, balancing delay path, and complementary OR gates in a block 2. The current mirror type’s structure provides a wide operating range, and stacked PMOS transistors in their complementary OR gate limit the leakage current [6].

Level shifters should satisfied the following condition,

1. Small area for sub threshold level conversions.
2. Low power consumptions in super threshold operation.
3. Balancing rising and falling delay in the operating Range.
4. Bidirectional level conversions.

Figure 4. Modified Wison Current Mirror based Level Shifter

III. POWER REDUCTION METHOD

Forced PMOS is main methods of leakage power reduction Techniques. In this method pull down networks is not modified. Pull up networks is only modified with the forced PMOS method.
An existing PMOS transistor is split into a two each transistor is having the Width/Length ratio of half compare with existing transistors. Consider a inverter as an example. By applying this forced PMOS methods to the inverter the power can be decreased from 2 pw to 1.75 pw. In these methods two PMOS transistors increased the delay in the current flow paths. So that power can be increased. Other leakage power reduction method is stacked method and a forced NMOS method.

Stack approach is one of the leakage power reduction methods, which forces a stack effect by breaking down an existing transistor into two half size transistors [9]. When the two transistors are turned off together, induced reverse bias between the two transistors results in leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach [10].

In forced NMOS approach if input is given low as compared to threshold voltage., then at the same time PMOS turns on and NMOS turns off and if input is given high at the gate terminal as compared to threshold voltage, then at the same time PMOS turns off and NMOS turn on. Here, the two NMOS transistors which increase the delay in the flow of the current which ultimately decreases the leakage power in the circuit [11].

IV. PROPOSED LEVEL SHIFTERS

In this section existing Level Shifters are modified by using the forced NMOS approach. Figure (5, 6, 7, 8) shows the conventional cross coupled method, current mirror based level shifters, Wilson current mirror based level shifters and modified. These level shifters were designed by using the Forced PMOS method. Power was reduced when comparing with existing level shifters.

In forced PMOS method pull up networks is only modified. Here existing PMOS transistor W/L ratio is 0.6u/0.4u proposed circuit was designed by splitting the existing PMOS transistors into two each having the W/L ratio of 0.45u/0.6u.

![Fig.5. Modified Conventional cross coupled level shifter](image-url)
Fig.6. Current mirror based level shifter using Forced PMOS

Fig.7. Wilson Current Mirror based level shifter using Forced PMOS

Fig.8. MWCM based level shifter using Forced PMOS

V. SIMULATION AND RESULT

Simulation results for proposed Level shifters is shown in Figure (9, 10, 11, 12) respectively. Waveform for modified conventional cross coupled level
shifters is shown fig.9. Input cross coupled voltage is 2.5v and output voltage is 0.22v. Current mirror based level shifters is also shift the voltage from 2.5v to 0.22v.

Wilson current mirror based level shifters are used to shift the voltages from 2.5v to 0.13v. Modified Wilson Current Mirror (MWCM) based level shifters are a bidirectional level shifter which is used to shift the voltage from 1v to 5v. Waveform for MWCM is shown in Figure 12.

![Waveform for conventional level shifter](image9)

**Fig.9. Waveform for conventional level shifter**

![Waveform for current mirror based level shifter](image10)

**Fig.10. Waveform for current mirror based level shifter**

![Waveform for Wilson current mirror based level shifter](image11)

**Fig.11. Waveform for Wilson current mirror based level shifter**
Simulation can be performed by using the Mentor Graphics. Mentor Graphics is one of the Electron Device Automation Tool.

In this tool Eldo Calibre are mainly used for the circuit simulation, LVS and DVS check.

![Fig.12. MWCM based level shifter](image)

**TABLE I. Power and Delay for Various Level Shifters without Forced PMOS Method**

<table>
<thead>
<tr>
<th>Level shifters</th>
<th>Power</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional Level Shifter</td>
<td>4.7923(mw)</td>
<td>0.1 ns</td>
</tr>
<tr>
<td>Current mirror based level shifter</td>
<td>4.3694(mw)</td>
<td>0.2 ns</td>
</tr>
<tr>
<td>Wilson current mirror based level shifter</td>
<td>1.7154(mw)</td>
<td>0.1 ns</td>
</tr>
<tr>
<td>Modified Wilson current mirror based level shifter</td>
<td>250.7207(nw)</td>
<td>0.3 ns</td>
</tr>
</tbody>
</table>

**Table. II. Power and Delay for Various Level Shifters with Forced PMOS Method**
### Table I

<table>
<thead>
<tr>
<th>Level shifters</th>
<th>Power</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional Level Shifter</td>
<td>1.8023(mW)</td>
<td>0.2 ns</td>
</tr>
<tr>
<td>Current mirror based level shifter</td>
<td>1.7877(mW)</td>
<td>0.5ns</td>
</tr>
<tr>
<td>Wilson current mirror based level shifter</td>
<td>1.0491(mW)</td>
<td>0.2ns</td>
</tr>
<tr>
<td>Modified Wilson current mirror based level shifter</td>
<td>250.0437(nW)</td>
<td>0.5ns</td>
</tr>
</tbody>
</table>

Table I and II shows the comparison of Normal level shifter design and level shifter design using Forced PMOS method. Comparing with existing and proposed method delay is slightly increased and power is decreased in proposed method.

**VI. CONCLUSION**

Conventional level shifter has the power dissipation of 4.8943 mw. The same circuits are designed by using a forced PMOS methods mean that time power is decreased from 4.6943mw to 1.8021mw. Likewise current mirror based level shifter, Wilson current mirror based level shifters, and Modified Wilson current mirror based level shifter is reducing the power consumptions from 4.3694mw, 1.7154mW and 250.7207nW to 1.7876mW, 1.0391mW and 250.0347nW.

**REFERENCES**


[10] Jun Zhou, Chao Wang, Xiu Liu, and at al., “A fast and energy-efficient level shifter with wide shifting range from sub-threshold up to I/O voltage”, in IEEE A-SSCC conf., 2013,


